10/726934

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Osamu Kobayashi

Attorney Docket No.: GENSP110

Patent: 6,992,987 B2

Issued: January 31, 2006

Title: ENUMERATION METHOD FOR THE LINK CLOCK RATE AND THE PIXEL/AUDIO CLOCK RATE

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on July 24, 2006 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Aurelia M. Sanchez

REQUEST FOR CERTIFICATE OF CORRECTION OF OFFICE MISTAKE (35 U.S.C. §254, 37 CFR §1.322)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Attn: Certificate of Correction

Certificate
AUG 02 2006
of Correction

Dear Sir:

Attached is Form PTO-1050 (Certificate of Correction) at least one copy of which is suitable for printing. The errors together with the exact page and line number where the errors are shown correctly in the application file are as follows:

SPECIFICATION:

1. Column 5, line 28, change "stream 10" to --stream 110--. This appears correctly in the patent application as filed on December 2, 2003, on page 11, paragraph 0015, line 6.

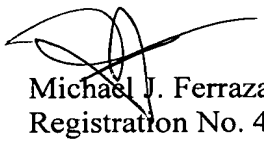
2. Column 7, line 36, change express" to --expressed--. This appears correctly in Amendment A as filed on August 19, 2005, on page 4, line 10.

3. Column 7, line 37, change "express" to --expressed--. This appears correctly in Amendment A as filed on August 19, 2005, on page 4, line 11.

Patentee hereby requests expedited issuance of the Certificate of Correction because the error lies with the Office and because the error is clearly disclosed in the records of the Office. As required for expedited issuance, enclosed is documentation that unequivocally supports the patentee's assertion without needing reference to the patent file wrapper.

It is noted that the above-identified errors were printing errors that apparently occurred during the printing process. Accordingly, it is believed that no fees are due in connection with the filing of this Request for Certificate of Correction. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. GENSP110).

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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[0015] For example, if the data stream 110 is an analog type signal, the an analog to digital converter (not shown) included in or coupled to the transmitter 102 will digitize the analog data which is then packetize by a packetizer that converts the digitized data stream 110 into a number of data packets 114 each of which will be transmitted to the receiver 104 by way of the virtual link 116. The receiver 104 will then reconstitute the data stream 110 by appropriately recombining the data packets 114 into their original format. It should be noted that the link rate is independent of the native stream rates. The only requirement is that the link bandwidth of the physical link 106 be higher than the aggregate bandwidth of data stream(s) to be transmitted . In the described embodiment, the incoming data (such as pixel data in the case of video data) is packed over the respective virtual link based upon a data mapping definition. In this way, the physical link 106 (or any of the constituent virtual links) does not, as does conventional interconnects such as DVI, carry one pixel data per link character clock.

[0016] In this way, the interface 100 provides a scaleable medium for the transport of not only video and graphics data, but also audio and other application data as may be required. In addition, the invention supports hot-plug event detection and automatically sets the physical link (or pipe) to its optimum transmission rate. The invention provides for a low pin count, purely digital display interconnect for all displays suitable for multiple platforms. Such platforms include host to display, laptop/all-in-one as well as HDTV and other consumer electronics applications.

[0017] In addition to providing video and graphics data, display timing information can be embedded in the digital stream providing essentially perfect and instant display alignment, obviating the need for features like "Auto-Adjust" and the like. The packet based nature of the inventive interface provides scalability to support

accordance with an embodiment of the invention, this master frequency (23.76 GHz) can be expressed as a function of four parameters A, B, C, and D as:

$$23.76\text{GHz} = 2^A \times 3^B \times 5^C \times 11^D \text{ Hz where}$$

A=10, B=3, C=7, D=1,

$$(23.76\text{GHz} = 2^{10} \times 3^3 \times 5^7 \times 11^1 \text{ Hz}).$$

This means that a pixel (or audio) clock rate can be expressed **as a subset of the master frequency** with **these** four parameters, A, B, C, and D **(where $A \leq 10$, $B \leq 3$, $C \leq 7$, $D \leq 1$) as**

$$\text{Pixel (or audio) clock rate} = 2^A \pm x\, 3^B \times 5^C \times 11^D.$$

It should be noted that since A is less than or equal to 10, A can be expressed in 4 bits, and since B is less than or equal to 3, B can be expressed using as 2 bits, C as 3 bits and D as 1 bit. ~~**A = 4 bits, B = 2 bits, C = 3 bits, and D = 1 bit.**~~

Please replace paragraph **[0025]** with the following:

Even for a link whose link rate (which is the serial link bit rate / 10 for a link that uses 10-bit character such as 8B/10B characters) may be different from the pixel clock rate, there is a benefit in defining the link rate with these four parameters, A', B', C', and D': The benefit is the simplicity in regenerating pixel/audio clocks from a link clock. For example, let's say the link rate is set as A' = 6, B' = 3, C' = 7, and D' = 0 **(i.e., $LR = 2^6 \times 3^3 \times 5^7 \times 11^0$)** and the corresponding link rate is 135MHz. However, suppose the pixel clock rate is set as A = 8, B = 3, C = 6, and D = 0 **(i.e., $PC = 2^8 \times 3^3 \times 5^6 \times 11^0$) (= and the corresponding pixel clock rate is** 108MHz~~)~~, then the pixel clock can be generated from link clock **by the following equation**

Pixel clock rate = (link rate) x ($2^{A-A'}$, $3^{B-B'}$, $5^{C-C'}$, and $11^{D-D'}$). For the above example,

(Pixel clock rate/Link rate) = $(2^8 \times 3^3 \times 5^6 \times 11^0)/(2^6 \times 3^3 \times 5^7 \times 11^0)$ or

Pixel clock rate = (Link rate) x $(2^2)x(3^0)x(5^{-1})x(11^0)$ = Link rate x (.8).

AUG 8 2006

PTO/SB/44 (10-96)
Approved for use through 6/30/99. OMB 0651-0033
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PT-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,992,987 B2

DATED : January 31, 2006

INVENTOR(S) : Osamu Kobayashi

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the Specification:

Column 5, line 28, change "stream 10" to --stream 110--.

Column 7, line 36, change express" to --expressed--.

Column 7, line 37, change "express" to --expressed--.

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